

Subt D²

CLEAN VERSION OF AMENDED CLAIMS

24. (twice amended) A semiconductor package comprising:

a substrate comprising a first surface, a second surface, a plurality of conductors and ball bonding pads on the first surface, and a bonding opening from the first surface to the second surface;

a semiconductor die having a first outline and a face on the bonding opening bonded directly to the second surface;

a first mask on the first surface comprising a plurality of via openings aligned with the ball bonding pads;

a second mask covering the second surface except in a die attach area defined by an opening through the second mask having a second outline substantially matching the first outline;

an adhesive layer between the die and the substrate in the die attach area bonding the face to the second surface; and

a plurality of wires placed through the bonding opening and wire bonded to the die and to the conductors.

25. (twice amended) The package of claim 24 further comprising an encapsulating material at least partially encapsulating the die and the second mask.

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26. (twice amended) The package of claim 25 wherein the adhesive layer comprises a filled adhesive.

27. (twice amended) A semiconductor package comprising:

a substrate comprising a first surface, a second surface, a plurality of conductors on the first surface comprising ball bonding pads and wire bonding pads, and a bonding opening from the first surface to the second surface;

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a semiconductor die having a first outline, the die comprising a face on the bonding opening bonded to the second surface;

a first mask on the first surface comprising a plurality of via openings aligned with the ball bonding pads and a first opening exposing the wire bonding pads;

a second mask substantially covering the second surface comprising a second opening having a second outline substantially matching the first outline to define an open die attach area on the second surface;

an adhesive layer between the die and the substrate in the open die attach area bonding the face to the second surface; and

a plurality of wires in the bonding opening wire bonded to the die and to the wire bonding pads.

28. (twice amended) The package of claim 27 further comprising a glob top in the bonding opening and on the first surface at least partially encapsulating the wires.

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29. (twice amended) The package of claim 27 wherein the first mask and the second mask comprise a photoimageable material.

30. (twice amended) A semiconductor package comprising:

a substrate having a first surface, a second surface and a bonding opening there through;

a plurality of conductors on the first surface comprising a plurality of ball bonding pads;

a first mask on the first surface comprising a plurality of via openings to the ball bonding pads;

a semiconductor die having a face on the bonding opening attached directly to the second surface;

a second mask covering the second surface except in a die attach area defined by an opening through the second mask having an outline substantially matching that of the face;

a plurality of solder balls in the via openings bonded to the ball bonding pads; and

a plurality of wires placed through the bonding opening and bonded to the die and to the conductors.

31. (twice amended) The package of claim 30 further comprising an encapsulating resin on the second surface at least partially encapsulating the die.

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32. (twice amended) The package of claim 30 further comprising a plurality of wire bonding pads on the conductors wire bonded to the wires and a second opening in the first mask exposing the wire bonding pads.

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33. (twice amended) The package of claim 30 further comprising a filled adhesive layer attaching the die to the substrate in the open die attach area.

34. (twice amended) A semiconductor package comprising:

a substrate comprising a first surface, an opposing second surface and a wire bonding opening from the first surface to the second surface;

a plurality of conductors on the first surface comprising wire bonding pads and ball bonding pads;

a first mask on the first surface comprising a plurality of via openings aligned with the ball bonding pads and a first opening exposing the wire bonding pads;

a semiconductor die aligned with the wire bonding opening and bonded face down to the second surface, the die having a first outline;

a second mask substantially covering the second surface and including an opening there through having a second

outline substantially matching the first outline to define an open die attach area on the second surface;

an adhesive layer between the die and the substrate in the open die attach area bonding the die directly to the second surface;

a plurality of wires placed through the wire bonding opening and bonded to the die and to the wire bonding pads; and

an encapsulating resin on the second surface at least partially encapsulating the die.

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35. (twice amended) The package of claim 34 further comprising a glob top in the wire bonding opening at least partially encapsulating the wires.

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36. (twice amended) The package of claim 34 wherein the adhesive layer comprises a filled epoxy.